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10/697,461	10/30/2003	Martin A. Cotton	8245.061	7982

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DUNLAP, CODDING & ROGERS P.C.
PO BOX 16370
OKLAHOMA CITY, OK 73113

EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,461	COTTON, MARTIN A.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *17-20,22 and 29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,21,23-28 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/03,6/04,8/04,*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, claims 1-16, 21, 23-28, and 30 in the reply filed on 25 August 2005 is acknowledged.

Specification

The disclosure is objected to because of the following informalities: There is no brief description of figure 6A.

Appropriate correction is required.

Claim Objections

Claim 1 is objected to because of the following informalities: Change "through hold" to --through hole--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by US 5,958,562 (Tsuji).

Tsuji discloses, referring primarily to figure 2B, a printed circuit board having a wiring connection structure for interconnecting wiring circuit traces on a plurality of circuit trace layers applied on a plurality of printed circuit board layers and electrically isolated there between by the printed circuit board layers and having a printed circuit board multi-layer structure, characterized by: a through hole (10) having a non-circular shaped cross section normal to a longitudinal axis of the through hole (see col. 3, lines 1-10) and having an interior wall that vertically extends through and intersects and exposes at least two wire circuit traces (7, 9) and having a plating of conductive material (8C) applied to the interior wall electrically connecting the at least two wire circuit traces [claim 1].

Claims 2, 9-12, 21, 23-26, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by US 5,828,555 (Itoh).

Itoh discloses, referring primarily to figure 2, a printed circuit board having an EMI shielding structure for shielding wiring circuit traces on a plurality of circuit trace layers applied on a plurality of printed circuit board layers and electrically isolated there between by the printed circuit board layers and having a printed circuit board multi-layer structure, characterized by: a trench (41) having a rim about an opening of the trench at a top printed circuit board layer and said trench extending through a plurality of printed circuit board layers to a grounding plane (32) exposing said grounding plane and said trench having an interior wall with a conductive plating material (53) applied over said interior wall and said trench having a length greater than two times a breadth of

said trench and wherein the trench extends completely around an area of the printed circuit board and wherein said conductive plating material electrically connects to said exposed grounding plane [claim 2].

Additionally, Itoh discloses, a printed circuit board having a reference plane structure for fixing a potential reference for a plurality of wiring circuit trace layers that are electrically isolated there between by a plurality of printed circuit board layers and having a printed circuit board layer with a main surface, characterized by: a wire trace circuit layer (32) applied to said main surface; a printed circuit board insulation layer (35) formed over said wire trace circuit layer; a reference plane (31) applied over the printed circuit board insulation layer; a trench (41) having an interior wall extending through and exposing the wire trace circuit layer, and the trench further extending through the insulation layer to the reference plane wherein the reference plane is exposed; and a conductive plating layer (51) on the interior wall electrically connects the wire trace circuit layer to the reference plane [claim 9], wherein the trench completely encompasses the wire trace circuit layer [claim 10], wherein the reference plane is fixed at a ground potential (see col. 4, lines 1-5) [claim 11], wherein the reference plane is fixed at a reference voltage (see col. 4, lines 1-5) [claim 12].

Also, Itoh discloses, referring primarily to figure 6, a printed circuit board having an EMI shielding structure for shielding a plurality of wire trace layers, characterized by: a printed circuit board layer having a wire trace (33B) applied thereto; an insulation layer (35); and a grounding plane (31); a first trench (41B-1) having an interior wall and forming a perimeter encompassing the wire trace and extending through the printed

circuit board layer and extending to the ground plane and exposing said ground plane; and an electrically conductive plating material (51) applied upon the interior wall of the first trench and electrically connecting to the exposed ground plane providing a perimeter shield for the trace [claim 21], further characterized by: a second trench (40A) having an interior wall and spaced a distance from the first trench such that the wire trace extends between the first trench and second trench, the second trench extending through the printed circuit board said ground plane, layer and extending to the ground plane exposing said ground plane wherein the interior wall of the second trench is plated with an electrically conductive plating material (52) electrically connecting to the exposed ground plane thereby providing a double trench shield [claim 23], further characterized by: an EMC sensitive track of conductive material (33) extending wholly within a perimeter defined by the first trench and disposed between a plurality of circuit board insulation layers through which the first trench extends [claim 24].

Moreover, Itoh discloses, a printed circuit board having an EMI shielding structure for shielding a plurality of wire trace layers, characterized by: a plurality of printed circuit board layers having a plurality of wire trace layers, each printed circuit board layer separated by an insulation layer and having a grounding plane layer; a first trench (41B-1) extending from a top printed circuit board layer to the grounding plane layer (32) and the first trench having; an electrically conductive plating (51) applied over an interior wall of the first trench and electrically connecting to the ground plane; and wherein the first trench completely surrounds at least an area of the printed circuit board layers [claim 25], further characterized by: a second trench (40B-1) disposed interior to

the first trench and said second trench extending substantially in parallel to the first trench; and the second trench having an electrically conductive plating (52) applied over an interior wall thereof electrically connecting to the ground plane and an EMC sensitive track (33B) extending in a printed circuit board layer positioned between the first trench and the second trench [claim 26].

Furthermore, Itoh discloses, a printed circuit board having an EMI shielding structure for shielding a plurality of wire trace layers, characterized by: a plurality of printed circuit board layers having a plurality of wire trace layers, each printed circuit board layer separated by an insulation layer (35) and having a grounding plane layer (32); a first trench (41B) extending from a top printed circuit board layer to the grounding plane layer and the first trench having an electrically conductive plating (51) applied over an interior wall of the first trench and electrically connecting to the ground plane; and a second trench (40B) disposed interior to the first trench and said second trench extending substantially in parallel to the first trench and the second trench having an electrically conductive plating (52) applied over an interior wall thereof electrically connecting to the ground plane; and at least two EMC sensitive tracks (33, 33B) extending in a printed circuit board layer positioned between the first trench and the second trench [claim 30].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3-8 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 3,571,923 (Shaheen) in view of Tsuji.

Regarding claims 3-8 and 28, Shaheen discloses, referring primarily to figures 6 & 7, a printed circuit board having a wiring connection structure for interconnecting at least two wire traces therein, characterized by: a first wire trace (4) applied to a main surface of a printed circuit board layer and having a first terminal landing pad (10) with a first through hole there through, and having an inner wall; a first insulation layer (2) formed over said first wire trace having a second through hole of identical cross sectional geometry to and vertically aligned with the first through hole and the second through hole having an inner wall; and a second wire trace (3) applied to the first insulation layer having a second terminal landing pad (9) with a third through hole having identical geometry to and vertically aligned with the first through hole and the third through hole having an inner wall; and wherein the inner wall of the first through

hole, the inner wall of the second through hole, and the inner wall of the third through hole are plated with an electrically conductive material (21) forming a plated hole that vertically intersects the first and second terminal pads and electrically connects the first wire trace and the second wire trace. Shaheen does not specifically state that the holes have a non-circular cross section [claim 3]. However, it is well known in the art to form through holes in non-circular shapes as evidenced by Tsuji (see col. 3, lines 1-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the holes in Shaheen with a non-circular cross section. The motivation for doing so would have been to allow flexibility of wiring layout. Furthermore, it has been held that more than a mere change of form is necessary for patentability. Span-Deck, Inc v. Fab-con, Inc. (CA 8, 1982) 215 USPQ 835. Similarly, since any shape is taught by Tsuji, the non-circular cross section may be irregular [claim 4], "U" shaped [claim 5], "L" shaped [claim 6], cross-shaped [claim 7]. Moreover, the modified invention of Shaheen teaches, wherein the first through hole has a shaped continuous curved cross section centered on a circumference diameter of a standard single diameter circular profile micro via and is wholly contained within or extends beyond the perimeter defined by the circumference diameter [claim 8], wherein the non-circular shaped cross section of the through hole is a cross, a "U", an "L'", an "E", a square, a rectangle, a "double cross" a star, an oval, a continuous curve, or an irregular shape (see col. 3, lines 1-10) [claim 28].

Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shaheen in view of US 6,037,547 (Blish).

Regarding claims 13-15, Shaheen discloses, a printed circuit board having a wiring connection structure, characterized by: a first wire trace 4 having a width and applied to a main surface of a printed circuit board layer and having a first terminal landing pad (10) and having a first through hole; a first insulation layer (2) formed over said first wire trace and having a second through hole having an inner wall and having identical geometry and orientation as the first through hole and vertically aligned with the first through hole; and a second wire trace (3) applied to the first insulation layer and having a second terminal landing pad (9) and having a third through hole having an inner wall and having identical geometry to the first through hole and aligned with the first through hole, and the inner wall of the first through hole, the inner wall of the second through hole, and the inner wall of the third through hole wherein are plated with an electrically conductive material (21) forming a plated hole which vertically intersects the first terminal pad and second terminal pad and electrically connects the first wire trace and the second wire trace. Shaheen does not specifically discloses that the first through hole has a non-circular cross section taken normal to a longitudinal axis of the first through hole and having an inner wall and with a major diameter and a minor diameter wherein the minor diameter is less than the width of the first wire trace and the major diameter is elongated and oriented along a longitudinal direction of the first terminal landing pad [claim 13]. However, Blish teaches using an elliptical via having an elliptical landing pad for electrical interconnection. Therefore, it would have been

obvious to one having ordinary skill in the art at the time of invention to use the elliptical via/pad taught by Blish as the through hole in the invention of Shaheen. The motivation for doing so would have been to have the ability to decrease the pitch of the via array, or provide improved routing of escape traces (see Blish abstract). Moreover, the modified invention of Shaheen teaches, wherein the major diameter is at least about twice that of the minor diameter (see Blish col. 6, lines 60-65) [claim 14], wherein the major diameter is at least about three times that of the minor diameter (see Blish col. 6, lines 60-65) [claim 15].

Likewise, regarding claim 16, Shaheen discloses, a printed circuit board having a wiring connection structure, characterized by: a first wire trace (4) having a first width and applied to a main surface of a printed circuit board layer and having a first terminal landing pad (10) an insulation layer (2) formed over said first wire trace and having a second through hole having an inner wall and having identical geometry and orientation as the first through hole and vertically aligned with the first through hole; and a second wire trace (3) applied to the insulation layer and having a second terminal landing pad (9) and having a third through hole having identical geometry to the first through hole and aligned with the first through hole, and wherein the inner wall of the first through hole, the inner wall of the second through hole, and the inner wall of the third through hole are plated with an electrically conductive material (21) forming a plated hole which vertically intersects the first terminal pad and second terminal pad and electrically connects the first wire trace and the second wire trace. Shaheen does not specifically

disclose that the landing pad has a second width which is greater than the first width and having a first through hole having a non-circular cross section taken normal to a longitudinal axis of the first through hole and having an inner wall and with a major diameter and a minor diameter and wherein the minor diameter is less than the second width and wherein the major diameter is greater than the first width and is oriented along a longitudinal direction within the first terminal landing pad [claim 16]. However, Blish teaches using an elliptical via having an elliptical landing pad for electrical interconnection. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use the elliptical via/pad taught by Blish as the through hole in the invention of Shaheen. The motivation for doing so would have been to have the ability to decrease the pitch of the via array, or provide improved routing of escape traces (see Blish abstract).

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji.

Tsuji discloses the claimed invention as described above with respect to claim 3, including a second plated through hole (see figure 2B) except Tsuji does not specifically state that the second plated through hole having a non-circular cross section which is different from the non-circular cross section of the first plated through hole [claim 27]. However, Tsuji teaches that the openings may have any shape (see col. 3, lines 1-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to make the cross-sections different shapes. The motivation for doing so would have been to differentiate the two holes via a visual inspection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents disclose EMI shielded PCBs:

US 4,845,311 Schreiber et al.,

US 5,522,132 Mattei.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

JCSN